ABSTRACT

A system for interconnecting a set of device chips by means of an array of microjoints disposed on an interconnect carrier is taught. The carrier is provided with a dense array of microjoint receptacles with an adhesion layer, barrier layer and a noble metal layer; the device wafers are fabricated with an array of microjoining pads comprising an adhesion layer, barrier layer and a fusible solder layer with pads being located at matching locations in reference to the barrier receptacles; said device chips are joined to said carrier through the microjoint arrays resulting in interconnections capable of very high input/output density and inter-chip wiring density.